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17EC63

Sixth Semester B.E. Degree Examination, Feb./Mar. 2022
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Describe with neat diagrams, the P-well fabrication process for CMOS. **(08 Marks)**

b. Discuss the working of nMOS enhancement mode transistor operation with necessary sketch. **(08 Marks)**

c. Compare CMOS and Bipolar technology. **(04 Marks)**

OR

2 a. With neat sketches explain nMOS fabrication steps. **(08 Marks)**

b. What are the advantages of BiCMOS process over CMOS technology? **(04 Marks)**

c. Explain the following:
i) Channel length modulation
ii) Noise margin. **(08 Marks)**

Module-2

3 a. Discuss the CMOS design style with a diagram. **(08 Marks)**

b. Draw the stick diagram for the following using CMOS logic:
i) $Y = \overline{A + B + C}$ ii) 2 input NAND gate. **(08 Marks)**

c. Draw the stick diagram for 2 input NOR gate using nMOS logic. **(04 Marks)**

OR

4 a. Define sheet resistance (R_s), standard unit of capacitance ($\square C_g$) and delay unit (τ). **(06 Marks)**

b. Calculate the on resistance for nMOS inverter with $R_{sn} = 10K\Omega$, $2_{pu} = 8$ and $2_{pd} = 1$. **(06 Marks)**

c. Obtain the expression for total delay for N-stages of nMOS and CMOS inverters interms of width factor f and delay τ. **(08 Marks)**

Module-3

5 a. Define regularity and define scaling. **(04 Marks)**

b. Derive the scaling factor for the device parameter:
i) Parasitic capacitance
ii) Channel resistance
iii) Gate delay. **(06 Marks)**

c. Implement the ALU functions like Ex-OR, Ex-NOR, And and OR operation with an adder write the block diagrams of a 4-bit ALU using adder element and explain. **(10 Marks)**

OR

6 a. Define scaling factors α and β. **(03 Marks)**

b. Design a 4 bit, 4×4 barrel shifter. Draw the nMOS implementation and explain in detail. **(09 Marks)**

c. Explain the carry select adder with a diagram. **(08 Marks)**

Module-4

7 a. With the block diagram, explain the operation of PLA showing AND, or plane. (08 Marks)
b. Discuss the architectural issues related to VLSI subsystem design. (06 Marks)
c. Explain physical design of FPGAS. (06 Marks)

OR

8 a. Discuss FPGA abstractions with a diagram. (08 Marks)
b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. (08 Marks)
c. Define and explain FPGA fabric. (04 Marks)

Module-5

9 a. Explain 3-transistor dynamic RAM cell with a suitable diagram. (08 Marks)
b. Discuss the requirements for system timing considerations. (08 Marks)
c. Write a short note on stuck-at fault. (04 Marks)

OR

10 a. Explain nMOS pseudo static RAM cell with schematic diagram. (08 Marks)
b. Explain logic verification principles in detail. (08 Marks)
c. Write a note on automatic test pattern generation. (04 Marks)

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